Waveform Architecture for Virtualized Ecosystems

# Virtualized SATCOM for Cloud Environments

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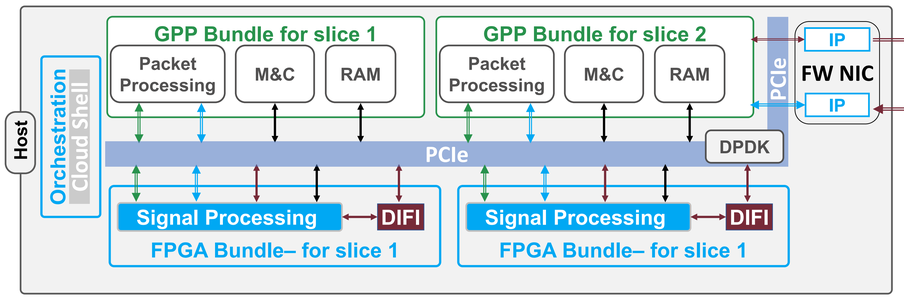
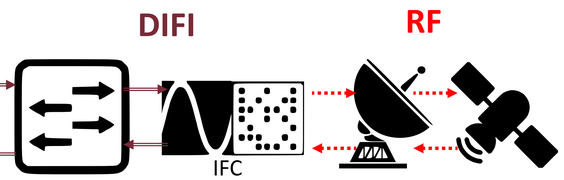
## Cloud Architecture




***Virtualized Modem Architecture***. GPP and FPGA bundles collaborate via PCIe to process DIFI streams, orchestrated through cloud-native control, enabling scalable multi-slice modem functions for RF connectivity.

- **GPP bundle** includes functions such as packet processing, monitoring and control (M&C), and RAM, supporting higher-layer functions.
- **FPGA bundle** executes real-time signal processing functions, interfaced with the Digital IF (DIFI) standard for transporting digitized signals.

Data flows through PCIe between GPP and FPGA bundles, with DPDK providing efficient packet transfer to the NIC for IP-based routing.

## Amazon EC2 F2 FPGA Configs

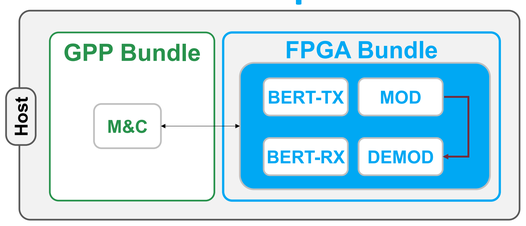
| Instance Type | FPGAs | vCPU | FPGA Memory (GiB) [HBM / DDR4] | Instance Memory (GiB) | Local Storage (GiB) | Network Bandwidth (Gbps) | EBS Bandwidth (Gbps) |
|---|---|---|---|---|---|---|---|
| f2.6xlarge | 1 | 24 | 16 / 64 | 256 | 1 × 940 | 12.5 | 7.5 |
| f2.12xlarge | 2 | 48 | 32 / 128 | 512 | 2 × 940 | 25 | 15 |
| f2.48xlarge | 8 | 192 | 128 / 512 | 2,048 | 8 × 940 | 100 | 60 |

| FPGA Model | Logic Cells | DSP Slices | Block RAM (Mb) | UltraRAM (Mb) |
|---|---|---|---|---|
| Virtex UltraScale+ VU9P | ~2.5 Million | 6,840 | 75.9 | 270 |

AWS F2 instances leverage the Xilinx Virtex UltraScale+ VU9P FPGA to deliver scalable compute, memory, and bandwidth for demanding signal processing workloads. In U.S. on-demand pricing, the f2.6xlarge is about $1.98 per hour, the f2.12xlarge about $3.96 per hour, and the f2.48xlarge about $15.86 per hour.

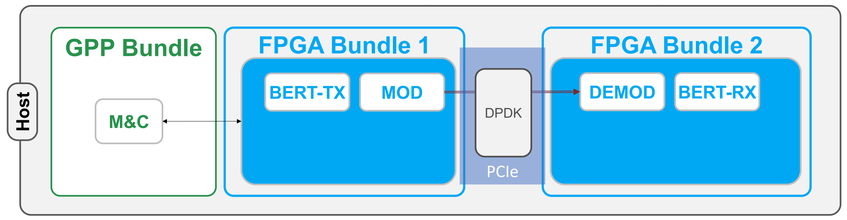
## Demonstration Configurations

### FPGA Loopback




The **FPGA loopback** configuration is used for testing and validation of modem functions in cloud environments. The GPP Bundle hosts M&C that oversee the FPGA Bundle components' operation metrics and configuration. Within the FPGA Bundle, the system includes a Bit Error Rate Tester transmitter (BERT-TX) and receiver (BERT-RX) alongside modulation (MOD) and demodulation (DEMOD) functions. The loopback path directly connects the MOD output to the DEMOD input, enabling end-to-end verification of waveform processing, error performance, and signal integrity without requiring external links.

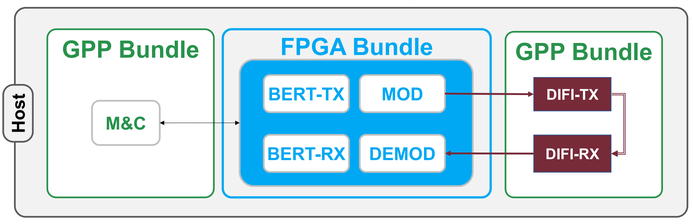
### Internal Fabric Loopback (Multiple FPGA)



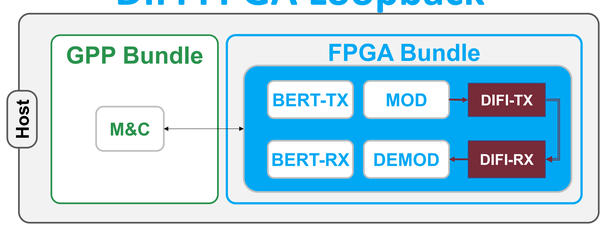

The **Internal FPGA Loopback** configuration interconnects multiple FPGA bundles through the PCIe fabric. **FPGA Bundle 1** generates and modulates a test signal using the BERT-TX and MOD blocks, while **FPGA Bundle 2** receives and demodulates the signal through the DEMOD and BERT-RX blocks. The transfer of data between bundles is managed by the Data Plane Development Kit (DPDK) over PCIe.

**DIFI loopbacks** provide a method to validate the interfaces between the FPGA and GPP bundles and test DIFI blocks. In the **DIFI GPP loopback**, digitized signals are passed from the FPGA modulation chain to DIFI transmit and receive blocks implemented on the GPP, confirming correct encapsulation and transport of IF data. In the **DIFI FPGA loopback**, DIFI transmit and receive functions are instead hosted within the FPGA bundle, allowing end-to-end validation of a hardware-accelerated DIFI path.

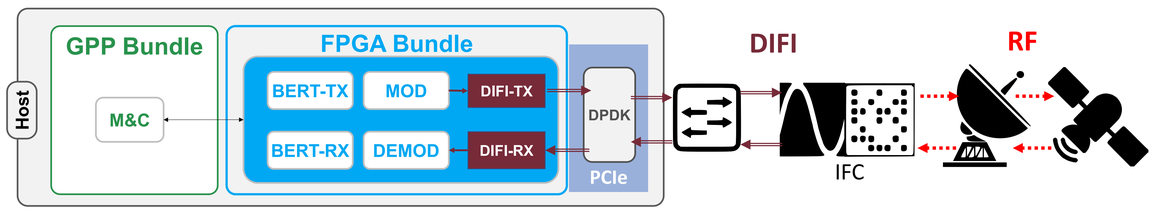
### DIFI GPP Loopback




### DIFI FPGA Loopback

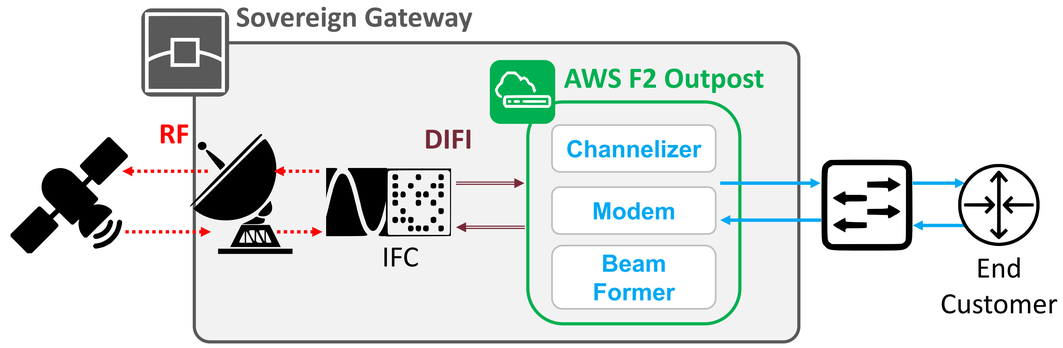



### Transponded Loopback



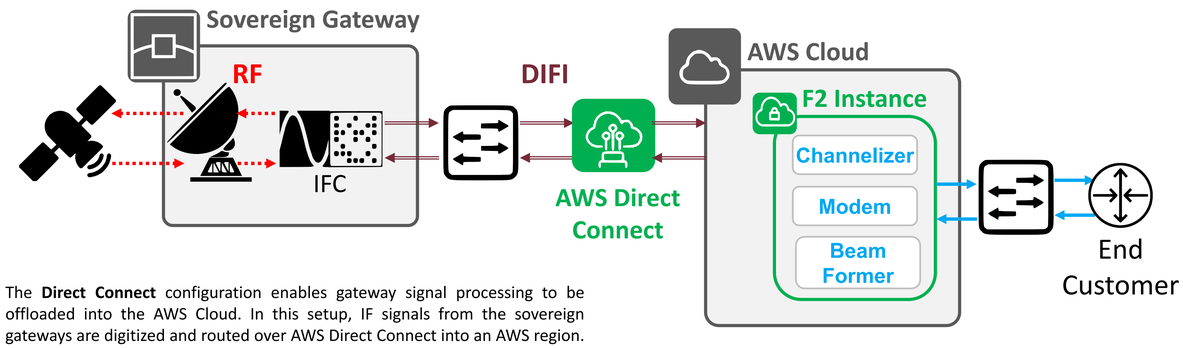

**Transponded Loopback** extends validation to external DIFI interfaces, enabling full end-to-end testing across RF paths. In this configuration, the FPGA bundle generates and modulates a test signal, which is packetized by the DIFI transmit block and passed through the PCIe/DPDK layer to an external RF front end. The returning RF signal is digitized, depacketized by the DIFI receive block, and routed back into the demodulation and BERT-RX chain. This setup verifies proper operation of the complete transmit–receive chain, including external DIFI transport and RF conversion, ensuring readiness for integration with real-world gateway and terminal systems.

### Proposed Outpost Configuration




Future Outpost configurations place **AWS F2 instances** directly at the operator's sovereign gateways, bringing cloud-based signal processing capabilities on-premise. By hosting channelization, modem functions, and beam forming locally, operators maintain low-latency access to critical waveform processing while still benefiting from the flexibility of cloud-native orchestration. This approach ensures that DIFI signals can be processed at the gateway before routing traffic to end customers, enabling efficient use of bandwidth and minimizing transport delays. The Outpost option complements the Direct Connect configuration by offering operators a hybrid model—keeping latency-sensitive processing close to the antenna while retaining the scalability and agility of cloud-managed infrastructure. Outpost instances will vary based on configuration and customer terms.

### Direct Connect Configuration




The **Direct Connect** configuration enables gateway signal processing to be offloaded into the AWS Cloud. In this setup, IF signals from the sovereign gateways are digitized and routed over AWS Direct Connect into an AWS region. Within the cloud, FPGA-enabled F2 instances host virtualized signal processing functions—including channelization, modem processing, and beam forming—executed on demand. By extending the gateway into the cloud region, operators can scale waveform and processing resources elastically while reducing dependence on on-premise hardware.

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