High-Performance Digital IF Modem for SATCOM

ATG has been awarded a Phase II SBIR from US Space Force (USSF) and the Space Development Agency (SDA) to develop a high-performance digital IF demodulator capability.

Project Objectives

- *Create a digital IF modem with efficient monitoring and control of data paths for the waveform.*
- *Achieve seamless communication between the host processor and the FPGA*
- *Demonstrate interoperability with a 3rd party IFC.*

ATG will utilize its COTS ADx-110/120 platform (Figure 1) for implementing our digital IF DVB-S2X demodulator. The proposed solution builds and enhances our existing digital IF Modem product. The existing product supports only a single demodulator, the proposed solution aims to support multiple digital IF DVB-S2X demodulators. By integrating a high-performance commercial DVB-S2X waveform, we can expand the capabilities of our existing product line and increase the throughput and signal-to-noise-ratio performance.

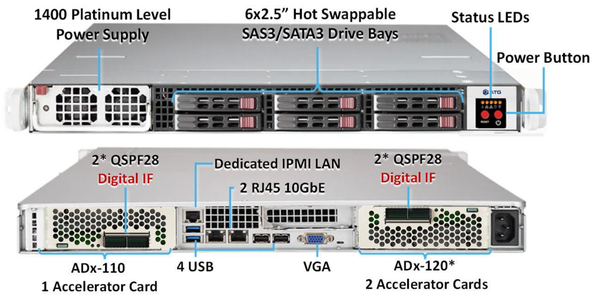

Figure 1 - *ADx-110/120 Digital IF Platform. The ADx-110/120 is the commercial platform for creating digital IF demodulators using FPGA accelerator cards and COTS server.*

The digital IF modem component performs waveform processing, and IF Converter (IFC) performs the RF processing. Digital IF architectures are a key enabler since they allow the digital IF modem to rely on common hardware by isolating specialized RF hardware into an IFC.

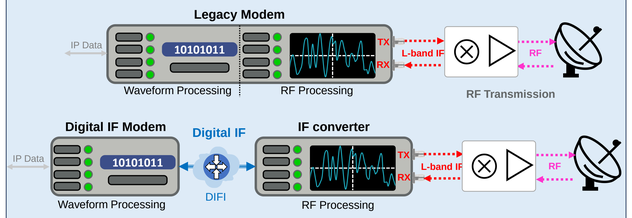

Figure 2 - *Digital IF separates legacy modem architectures into the digital IF modem and IF converter.*

Removing purpose–built RF hardware allows digital IF modem development on common computing hardware and jump to virtualization as the basis for terminal agility and flexibility.

Figure 3 illustrates the components to be developed. Specifications for the digital IF demodulator are captured in Table 1. Our solution will use an system on a chip architecture, which uses a embedded processing and FGPA in the same piece of silicon.

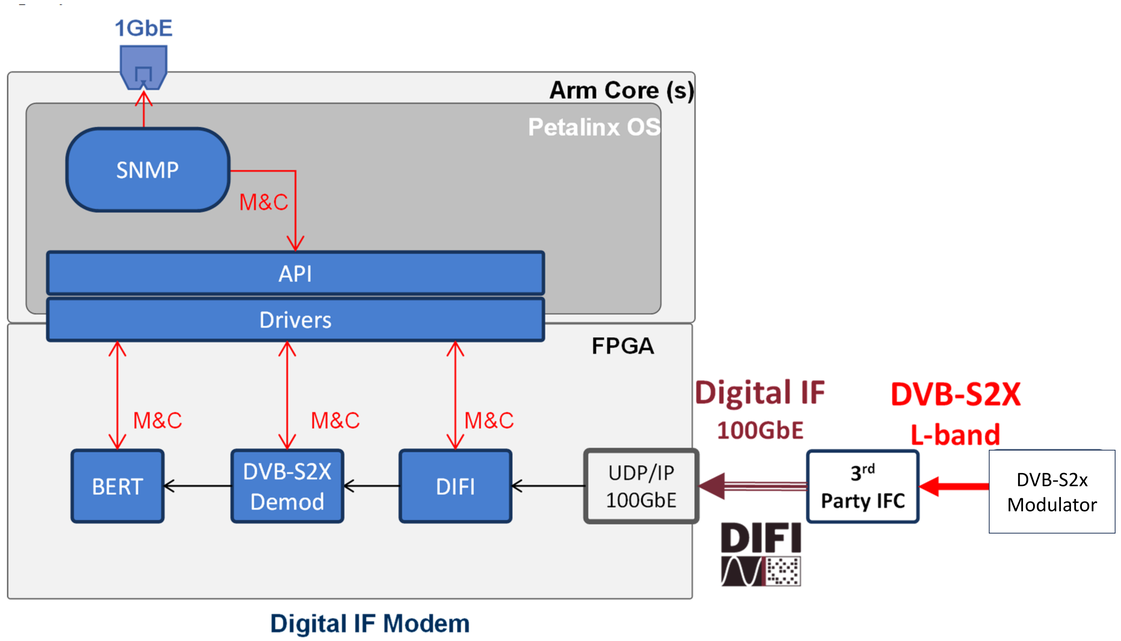

Figure 3 – *High Performance Digital IF Modem Design*

Table 1: ADx 110/120 Specifications

Digital IF Interfaces	
Digital IF Physical – ADx-110: 2* QSFP28 – ADx-120*: 4 QSFP28 **Digital IF MAC** – 100*/40*/10 GbE	**Digital IF Data Transport** – IEEE 4900-2022: DIFI V1.1 **Sampling** – 4*-16 bits per sample – Up to 125* Msamples/s
Mechanical & Power	
1RU: 17.2 x 1.7 x 28.5" (437 x 43 x 724 mm)	ADx-110 *153 W Nominal ADx-120 *165 W Nominal
Management Interfaces	
Web GUI, REST API	Dual RJ45 10 GbE Ports
Computing	
Processor: Intel® Xeon® 1.9GHz 3204 6-Core Processor w/ Intel Virtualization Technology	
RAM: 32 GB DDR4	**Disk Space:** 480 GB
DVB-S2X: 4-8 Waveform Capable*	
Modulation: QPSK, 8PSK, 16APSK, 32APSK, 64APSK, 128APSK, 256APSK **Symbol Rates:** 1-120* MSymbols/s **Roll Off:** 0.05 - 0.25 @ 0.05	

* Indicates Objective Specifications

Project Tasks:

Task 1: Develop FPGA Board Support Package (BSP)
- Integrate 100G Ethernet Core
- Integrate UDP/IP Core
- Integrate PCIe Gen3 Core
- Integrate GPIO and User control logic

Task 2: Waveform Integration with Control Logic
- Develop Netlist and Integrate Waveform onto FPGA

Task 3: Software Driver and UI Development
- Implement control framework for waveform management and control
- SNMP support

Task 4: Digital IF Interface
- Integrate DIFI v1.1 Core between waveform and Ethernet
- Develop new synchronization logic based on DIFI v1.2

Task 5: Test and Demonstration
- Test Waveform performance and DIFI packet compliance
- Test UPD/IP Ethernet frames
- Demonstrate DIFI interoperability with al least one 3rd party IFC

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