CLOSING THE TIMING LOOP WITH DIGITAL IF 1.2

MILCOM 2023

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ARKA

THE ISSUE

REAL-TIME SAMPLES PRODUCED AND CONSUMED BY INDEPENDENT DEVICES

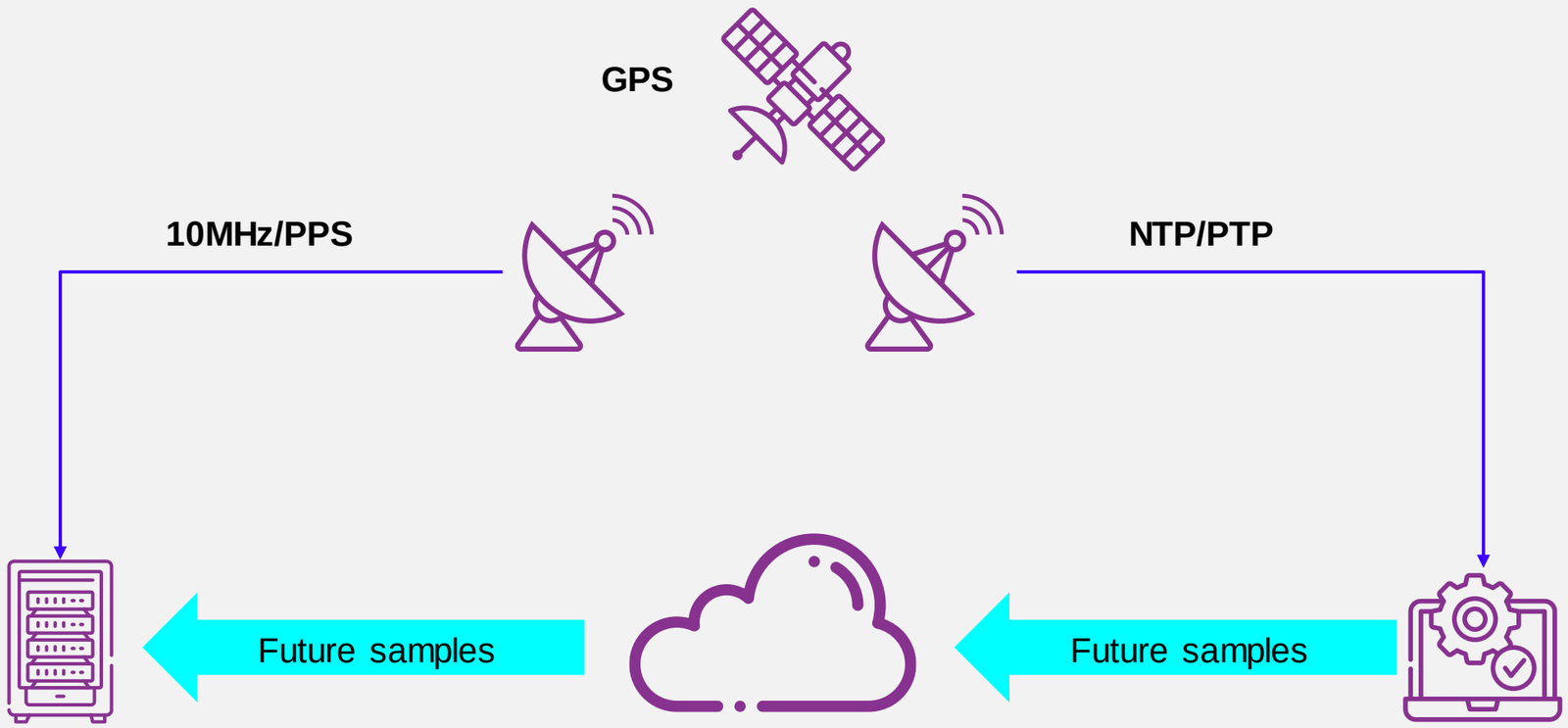
- Transmission over the network means that arrival times are delayed / jittered from transmit times.
  - No amount of buffer can solve a long-term average rate difference.
- Average long-term rate error must be 0.
- Buffer can solve errors in jitter / delay / burst that are cumulatively smaller than the buffer size.
- Large buffer depths can absorb larger errors but introduce larger latencies which can be unacceptable.

The problem is only hard when the sink is the reference for the sample rate:

- e.g. Software modem transmitting to digitizer for output to DAC

THE SIMPLE ANSWER

CLOSE THE LOOP THROUGH GPS



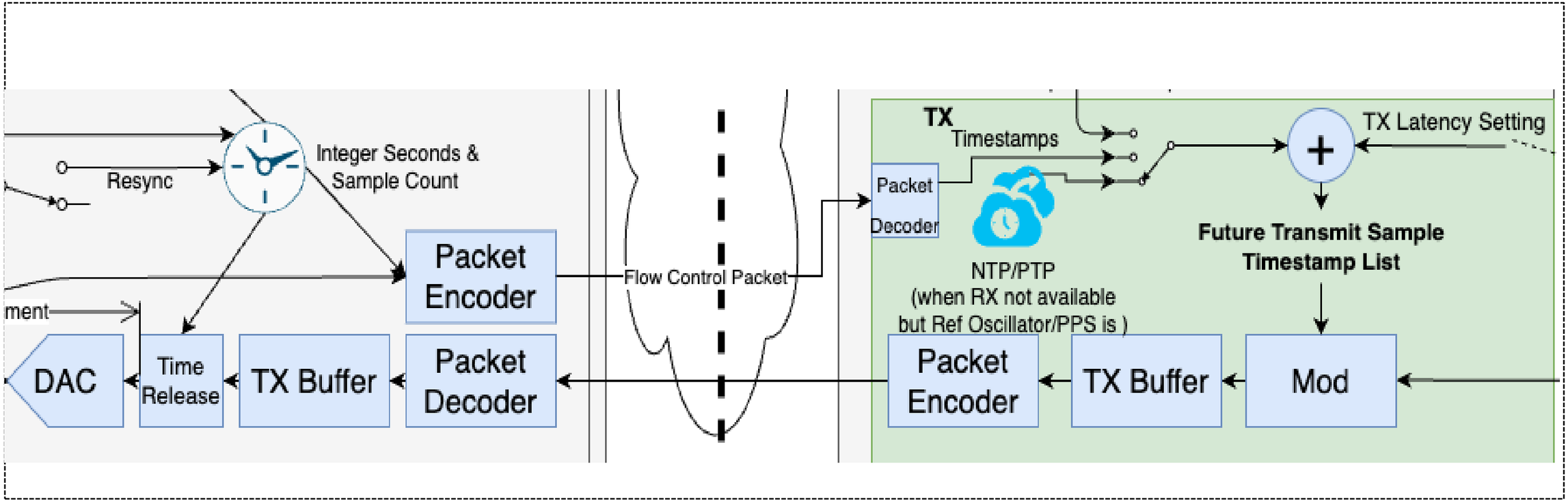
WHEN SIMPLE DOESN'T WORK

NO EXTERNAL LOOP

- Take away the reference at either end and now the potential for a rate mismatch occurs.
- We could enumerate all sorts of combinations of missing references but the solution for the worst case works for all of them.
- Worst case:
  - Isolated DAC running on a local oscillator with no idea of the actual UTC TOD.
  - Software sample source running on a computer with no access to NTP and the time set incorrectly

DIRECT LOOP CONCEPT

DIAGRAM FOR DISCUSSION



RULES FOR TIMESTAMPS

MAKING PACKETS THAT ARE “SENDABLE”

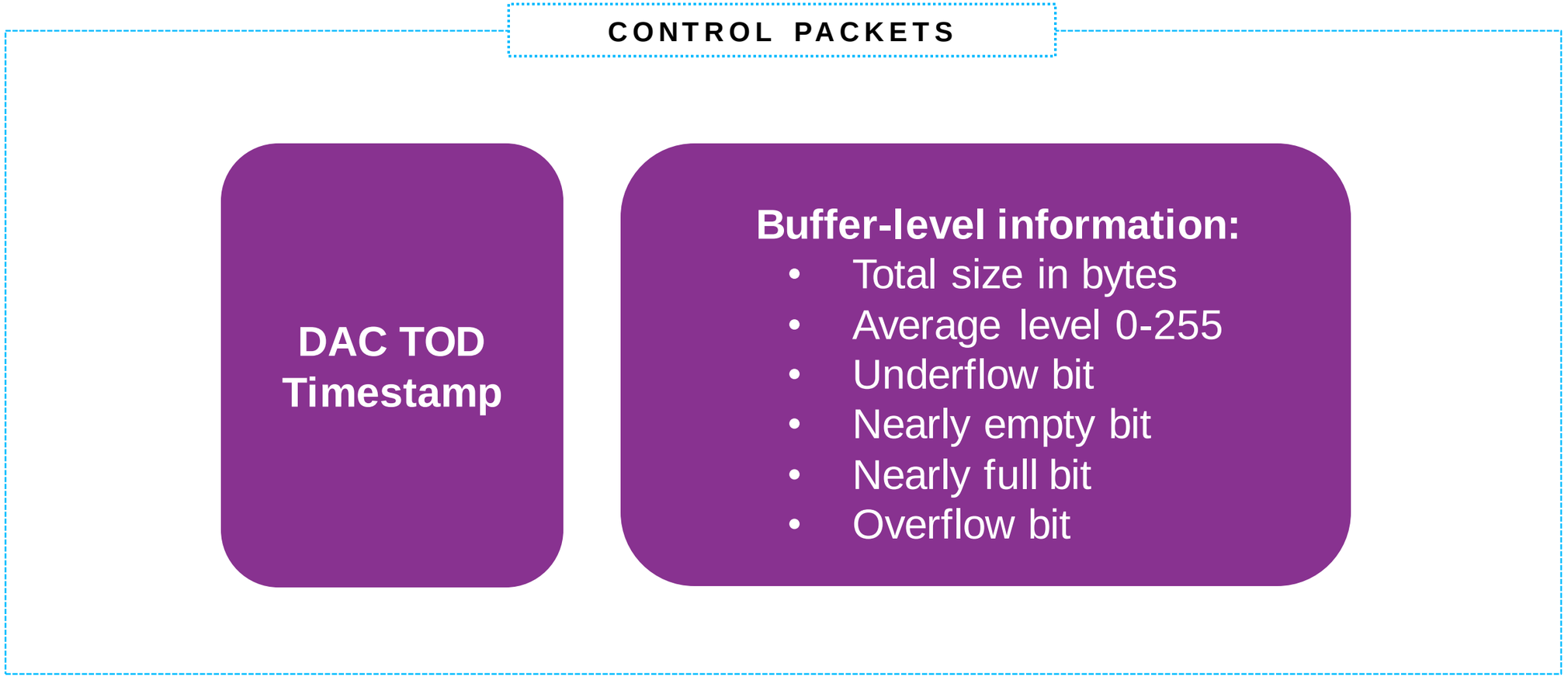
1. Producing valid future DAC timestamps is possible if they are always mathematically related to the present DAC time

2. As long as the timestamps are always predictable from a single valid timestamp and the sample rate, this is easy.

3. Timestamps should be mathematically perfect:
   - The owner of the clock (DAC) may form constantly changing opinions about the relationship between a TOD source (IRIG) and the sample clock
   - To make the timestamps predictable, it should only “resync” or cause a discontinuity in the DAC clock TOD on startup or on resync command.
   - Between resyncs, the source can always predict future DAC timestamps based on its current estimate of the DAC TOD and some simple math.

CONTROL PACKETS

A STREAM OF SYNCHRONIZATION INFORMATION



SOURCE ESTIMATING TOD AT THE SINK

SIMPLE ALGORITHM

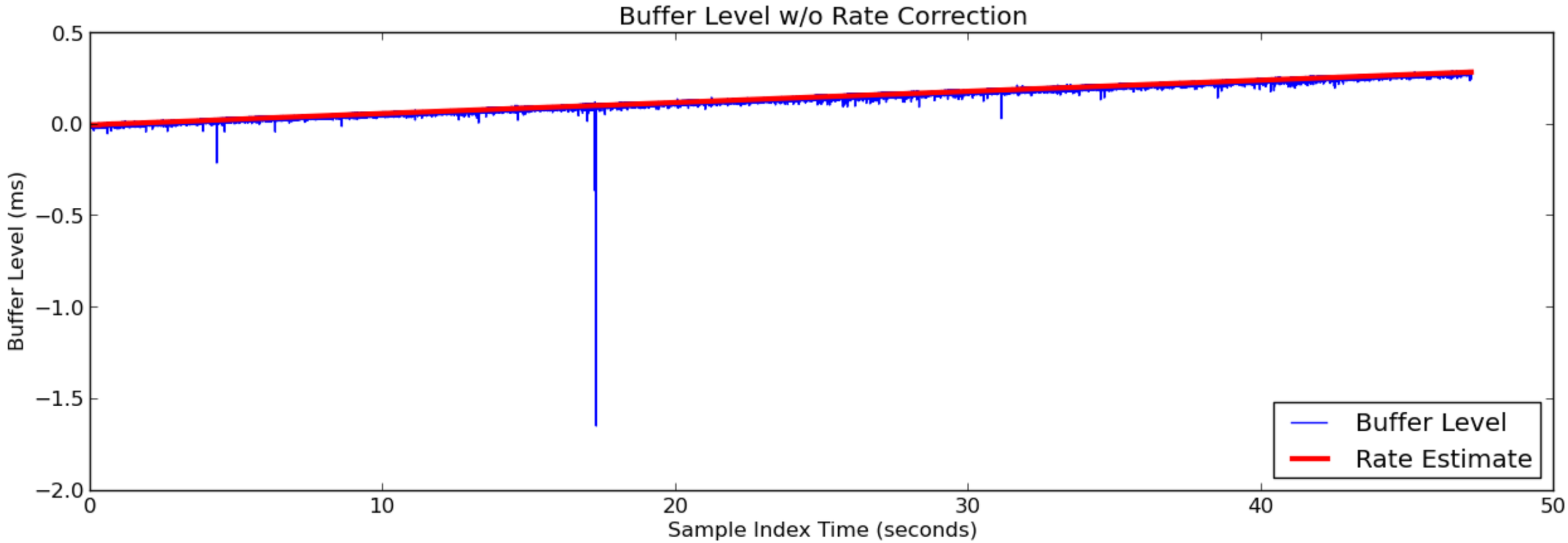
- Timestamp all arriving DAC TOD control packets with a local monotonic clock time.
- Save the delta between the embedded DAC TOD and the locally applied monotonic timestamp.
- When DAC TOD is needed at source for sample release, use monotonic + delta.
- Update delta on each control packet.

PROBLEMS

- Input network jitter is carried through as jitter in release times.
- Additional jitter occurs on the way to the DAC.
- Any rate differences manifest as steps in the value of delta and result in steps in the interpacket output delays.

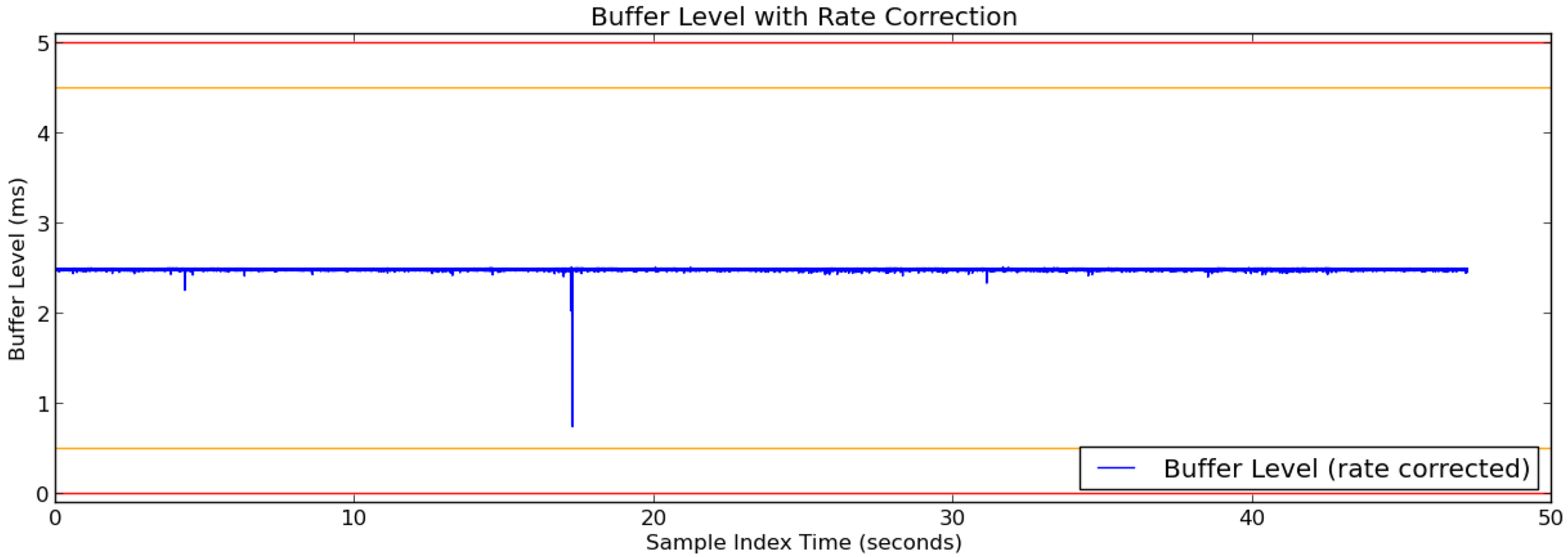
EXAMPLE FROM THE WILD

BUFFER LEVEL DRIFT DUE TO SAMPLE RATE MISMATCH



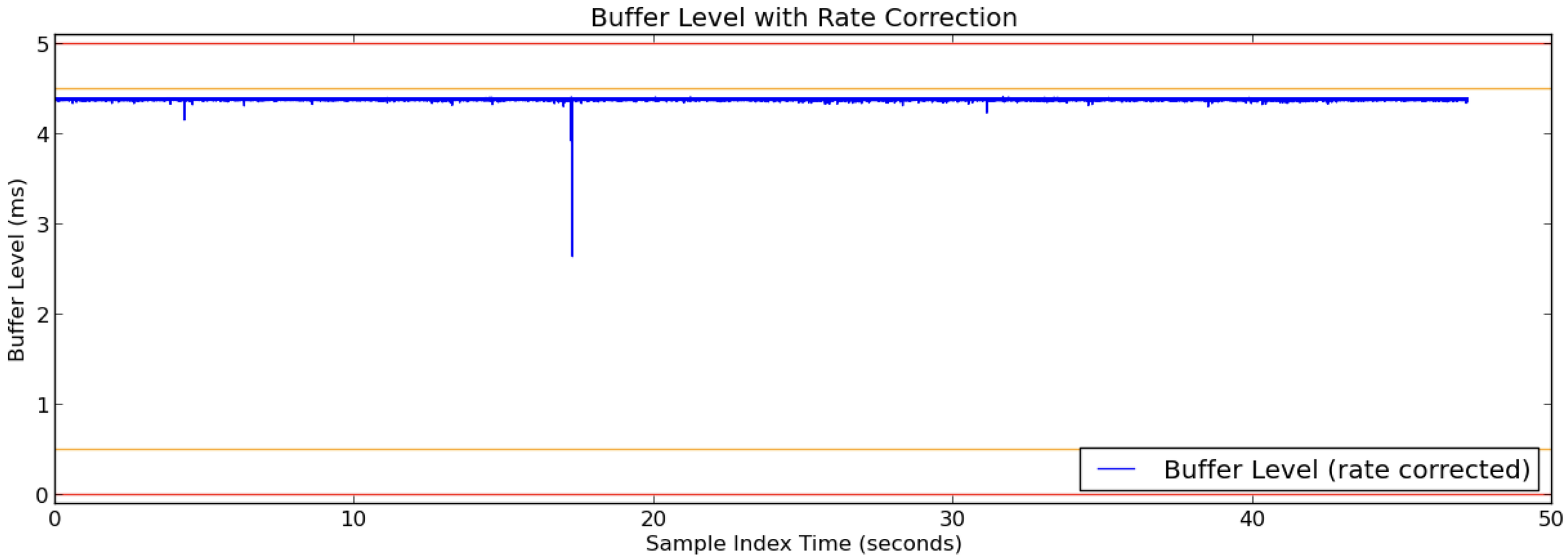
BUFFER DEPTH FROM THE REAL EXAMPLE

TARGET 50% BUFFER FULLNESS AVERAGE – SIMPLE / OBVIOUS ANSWER



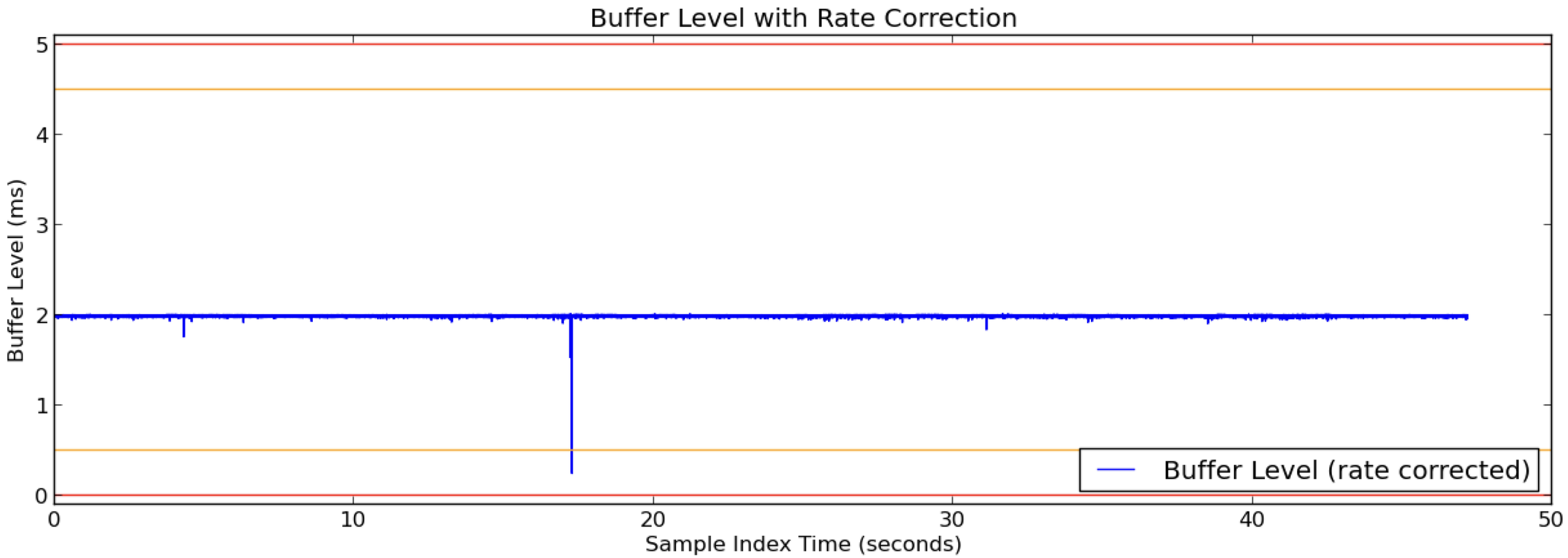
BUFFER DEPTH FROM THE REAL EXAMPLE

TARGET SOME "NEARLY FULL" WITH 0 OVERFLOW – MINIMIZE CHANCE OF UNDERFLOW



BUFFER DEPTH FROM THE REAL EXAMPLE

TARGET SOME "NEARLY EMPTY" WITH 0 UNDERFLOW – MINIMIZE LINK LATENCY



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THANK YOU FOR COMING!

QUESTIONS?

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