EXAMPLE

BUFFER LEVEL DRIFT DUE TO SAMPLE RATE MISMATCH



TARGET 50% BUFFER FULLNESS AVERAGE - SIMPLE / OBVIOUS ANSWER



TARGET SOME "NEARLY FULL" WITH 0 OVERFLOW - MINIMIZE **CHANCE OF UNDERFLOW**





DGTAL F12 SYNCHRONIZATION FEATURES

THE ISSUE

Real-time samples produced & consumed by independent devices:

- Transmission over network means that arrival times are delayed / jittered from transmit times.
- No amount of buffer can solve a long-term avg. rate difference.
- Buffer can solve errors in jitter / delay / burst that are cumulatively smaller than buffer size.
- Large buffer depths can absorb larger errors but introduce larger latencies.

Problem is only hard when the sink is the reference for the sample rate.

• Software modem transmitting to digitizer for output to DAC.



ESTIMATING TOD AT THE SINK -----

Linear Regression

- Timestamp all arriving DAC TOD control packets with a local monotonic clock time. • Perform a linear regression to determine offset & rate difference between DAC TOD &
- local monotonic time.
- When DAC TOD is needed at source for sample release, use monotonic * rate + delta.
- Update linear regression on each control packet.
- Real data shows asymmetric jitter, which can bend or offset the estimated line. A nuanced approach can remove outliers before estimating the slope.

Modem (SW)	
RX	
Packet RX Buffer Demod	User Data
Sample Timestamps	
TX Timestamps Packet Decoder NTP/PTP (when RX not available but Ref Oscillator/PPS is) TX Latency Setting Future Transmit Sample Timestamp List	Chosen to produce adeq Digitizer TX Buffering with worst case SW/netw jitter and delay. Constant for entire TX str
Packet TX Buffer Mod	User Data











EXAMPLE

TARGET SOME "NEARLY EMPTY" WITH 0 UNDERFLOW - MINIMIZE LINK LATENCY

	Buffer Level wit	h Rate Correction		
		1	1	
· · · · · · · · · · · · · · · · · · ·				
			— Buffer Level (rate o	orrected)
10	20 Sample Index	30 Time (seconds)	40	

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TRACKING STEPS

SWITCHING NETWORK PATHS OR DIGITIZERS